CLAIMS

1. In an integrated circuit (IC) having at least one fault to be tested by fault simulation using at least one test, each of said tests including at least one input test vector, a method for improving the efficiency of the fault simulation comprising the steps of:

a) performing a good machine simulation on said IC with said at least one test to obtain values of each internal node of said IC;

b) based on said good machine simulation, identifying faults in said IC that are potentially tested by said at least one test;

c) with said at least one test, performing a fault simulation on said faults that were identified as potentially tested; and

d) repeating steps a) through c) for each of said at least one test

2. The method as recited in of claim 1, wherein step b) further comprises backtracing from each observable node, said backtrace through each of said internal nodes being based on said fault-free circuit simulation and being limited to paths along which a faulty value has a possibility of propagating to said observable node.

3. The method as recited in claim 1, wherein said tests are generated by a test generator.

4. The method as recited in claim 1, wherein said fault-free-circuit simulation is performed by a logic simulator.

5. The method as recited in claim 1, wherein said fault simulation is performed by a hardware fault simulator.

6. The method as recited in claim 2, wherein the observed results of said test further limit the number of faults requiring processing by said fault simulation by starting said backtraces from only observable nodes wherein a fault was detected.

7. The method as recited in claim 1, wherein said IC comprises memory elements that are selected from the group that includes latches, flip-flops, random-access-memories (RAMs), and read-only-memories (ROMs) embedded in said IC.

8. In an integrated circuit (IC) having at least one fault to be tested by fault simulation using at least one test, each of said tests including at least one input test vector, a method for improving the efficiency of the fault simulation comprising the steps of:

a) performing a good machine simulation on said IC with said at least one test to obtain values of each internal node of said IC;

b) based on said good machine simulation, identifying faults in said IC that are blocked by said at least one test from being observed at an observable point of said IC;

c) with said at least one test, performing a fault simulation on said faults that were identified as not being blocked; and

d) repeating steps a) through c) for each of said at least one test.

9. A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method for improving the efficiency of a fault simulation of an integrated circuit (IC) having at least one fault to be tested by the fault simulation using at least one test, each of said tests including at least one input test vector, said method steps comprising:

a) performing a good machine simulation on said IC with said at least one test to obtain values of each internal node of said IC;

b) based on said good machine simulation, identifying faults in said IC that are blocked by said at least one test from being observed at an observable point of said IC;

c) with said at least one test, performing a fault simulation on said faults that were identified as not being blocked; and

d) repeating steps a) through c) for each of said at least one test

10. A computer program product comprising:

a computer usable medium having computer readable program code means embodied therein for improving the efficiency of a fault simulation of an integrated circuit (IC) having at least one fault to be tested by said fault simulation using at least one test, each of said tests including at least one input test vector, the computer readable program code means in said computer program product comprising:

a) computer readable program code means for causing a computer to perform good machine simulation on said IC with said at least one test to obtain values of each internal node of said IC;

b) computer readable program code means for causing the computer to identify faults in said IC that are blocked by said at least one test from being observed at an observable point of said IC, based on said good machine simulation;

c) computer readable program code means for causing the computer to perform a fault simulation on said faults that were identified as not being blocked with said at least one test; and

d) computer readable program code means for causing the computer to repeat steps a) through c) for each of said at least one test.